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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,347	KIMURA, HAJIME	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 46-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-16* is/are allowed.

6)☒ Claim(s) *1-6 and 47-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-22-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 12-01-05 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitations " a driving period", " a precharging period", " a programming period" in claims 1-4, " a first precharging period", "a third current", "a second precharging period", " a third potential" in claim 4 are not disclosed in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6, and 47-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the recitation "a transistor which supplies a first current to a load in a driving period; and a circuit for making a potential of a gate terminal of the transistor at a first potential by flowing a second current to the transistor in a precharging period, and for making the potential of the gate terminal of the transistor at a second potential by flowing the first current to the transistor in a programming period" is indefinite because of the following reasons:

- it is not clear what the recitations " driving period", " a first potential", " a precharging period" and " a programming period", " a first current", "a second current" are meant by.

- it is not clear what is the "a transistor" in the drawing and how it can supply " a first current" to the load in a driving period.

-the recitation "a circuit for making a potential of a gate terminal of the transistor at a first potential by flowing a second **current** to the transistor in a precharging period" on lines 4-6 is confusing because it is not clear how by flowing a second current to the transistor, the voltage at the gate can be at the first potential. It is not clear what part of the transistor the "second current" is flowed to.

- it is not clear what the recitation "for making the potential of the gate terminal of the transistor at a second potential by flowing **the first current** to the transistor in a precharge programming period" on lines 6-7 is confusing. On line 3 of the claim, the "first current" is the current that drive the load. On line 7 "the first current" is the current used to generate the "second potential" applied to the gate of the transistor in a programming period. Therefore, it is not clear as to the "first current" on line 7 is the same or different than the "first current" on line 3. The same rationale is applied to claims 2-4. The Applicant is requested to show which drawing the circuit of claims 1-4 reads on.

Claim 4 is indefinite because it is confusing. The Applicant is requested to show the "first current", " the second current", "the third current", " the first potential", " the second potential", "the third potential" and to explain what are "the driving period", "the first precharging period", " the second precharging period" and the "programming period". The Applicant is requested to show which drawing the circuit of claim 4 reads on.

Regarding claim 47, the recitation "generating at a gate terminal of a transistor a first voltage required for the transistor to flow a **first current** by supplying the **first current** to the transistor" on lines 4-5 is indefinite because it is confusing. As understood by the examiner, The "first current" is the current flowing through the drain-source of the transistor thus; in order to flow a first current through a transistor, a first voltage is needed to supply to the gate of that transistor. The recitation "generating at the gate terminal of the transistor a second voltage required for the transistor to flow a second current by supplying the second current to

the transistor" on lines 7-8 is indefinite for the same reason. The recitation "supplying the second current to a load after generating the second voltage" on lines 10 is indefinite because it is not clear how to "supply the second current to a load after generating the second voltage". The Applicant is requested to show which drawing, the limitations of claim 47 reads on.

Regarding claim 49, the recitation "generating at a gate terminal of a transistor a first voltage required for the transistor to flow a **first current** by supplying the **first current** to the transistor" on lines 4-5 is indefinite for the same reason above. The recitation "generating at the gate terminal of the transistor a second voltage required for the transistor to flow **a second current**, by supplying **the second current** to the transistor after generating the first voltage" on lines 7-9 has the same 112, 2nd problem. The recitation "generating at a the gate terminal of the transistor a third voltage required for the transistor to flow **a third current** by supplying **the third current** to the transistor after generating the second voltage" on lines 11-13 has similar 112, 2nd problem. The Applicant is requested to show which drawing, the limitations of claim 49 reads on and to show the first, second and third currents in the drawing and to show how to generate them.

Regarding claim 51, the recitation "wherein the circuit makes a potential of a gate electrode of the transistor at a predetermined potential by electrically connecting the second current source and the any one of the source region and the drain region of the transistor" on lines 8-10 is indefinite because it is misdescriptive. It is not clear why by connecting the drain/source of a transistor to a current source can make the gate of that transistor connected to predetermined potential. Explanation is required.

Claims 5, 6, 48, 50, 52 and 53 are indefinite because of the technical deficiencies of claims 4, 47, 49 and 51.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 47-51 are rejected under 35 U.S.C. 102(b) as being anticipated by Herrera (USP. 6,525,574).

Regarding claims 1-4, figure 3a and 3b show a semiconductor device comprising: a transistor (300) supplying a first current when switch (340) closes, a circuit (320, 350) when switch (350) closes the gate of transistor (300) is precharged for generating a second current. When capacitor (320) is fully charged, a third current will flow and transistor (300) is in "a programming mode".

Regarding claims 47 and 48, figure 3a and 3b show a driving method comprising the steps of generating at a gate terminal of a transistor a first voltage required for the transistor to flow a first current by supplying the first voltage to the transistor (switch 340 closes); generating at a the gate terminal of the transistor a second voltage required for the transistor to flow a second current by supplying the second voltage to the transistor (switch 350 closes to precharge capacitor 320); supply the second current to load (310) when switch (340) opens and switch (350) closes. The first current is larger than the second current because the first current is supplied directly from the bias source (Vbias).

Regarding claims 49 and 50, figure 3a and 3b show a driving method comprising: generating at a gate terminal of a transistor (300) a first voltage (switch 340 on, 350 off) required for the transistor to flow a first current by supplying the first current to the transistor; generating at the gate terminal of the transistor a second voltage (switch 340 off, 350 on) required for the transistor to flow a second current, by supplying the second voltage to the transistor after generating the first voltage when capacitor (320) is precharging; generating at a the gate terminal of the transistor a "third voltage" required for the transistor to flow a third current by supplying the third current to the transistor after generating the second voltage; and supply the third current to the load (310) when capacitor (320) is fully charged. The first current is larger than the second current because the first current is supplied directly from the bias source (Vbias).

Regarding claim 51, figure 3a and 3b show a semiconductor device comprising: a load (310), a transistor (300), a first current source (335), a second current source (330), the "circuit" is switch (350), the circuit connects the gate of transistor (300) to the current source (335) or (330).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 52 and 53 are rejected under 35 U.S.C.103 (a) as being unpatentable over Herrera (USP. 6,525,574).

Regarding claims 5, 6, 52 and 53 figures 3 and 3b of Herrera includes all the limitations of these claims except for the limitation that the device provides current to drive a display element, a signal line. However, when the circuit of Herrera can drive a load, it can provide current to drive other loads such as a display element, a signal line etc..

Allowable Subject Matter

Claims 7-16 are allowed.

Claims 7-16 are allowed because the prior art of records (USP. 6,710,995) fails to teach or suggest a semiconductor comprising: a load, a constant current source, first, second and third power source lines, first and second transistors and first, second and third switches connected as called for in claim 7. Therefore, claims 7-16 are presently allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory

period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
02-03-06

TUAN T. LAM
PRIMARY EXAMINER